IN THE CLAIMS:

The state of the claims as pending are as amended after the entry of an Examiner's Amendment dated August 23, 2005. Please amend claims 1, 2, 14, and 16-18 as follows:

1. (Currently Amended) A programmable frame splitter, comprising:

a plurality of programmable routers connected to a communication line, each of said routers having logic to control loading and startup of said routers, and logic to specify which bits of a frame of serial data is passed to an output of each of said routers; and

a plurality of field processing units to receive a bit clock out signal from each of said routers and serial data from the communication line, wherein each of said field processing units splits the frame of serial data into component fields and performs processing on the component fields, wherein [[the]] a control unit receives a bus signal, a frame start signal, and a bit-clock-in signal.

2. (Currently Amended) The programmable frame splitter according to claim 1, wherein the logic controlling the loading and startup of said routers is contained in [[a]] the control unit.

3. (Cancelled)

4. (Original) The programmable frame splitter according to claim 1, wherein the component fields include voice, video, and data.

5. (Original) The programmable frame splitter according to claim 1, wherein the logic to specify which bits of the frame of serial data is passed to the output of each of said routers is implemented utilizing at least one memory device.

6. (Original) The programmable frame splitter according to claim 5, wherein the logic is implemented with a N x 1 memory device and an address counter, where N is a number of bits equal to the largest possible frame size.

7. (Original) The programmable frame splitter according to claim 5, wherein the logic is implemented with a N bit register and a N bit shift register, where N is a number of bits equal to the largest possible frame size.

8. (Previously Presented) A programmable frame splitter, comprising:

a plurality of programmable routers connected to a communication line, each of said routers containing logic to specify which bits of a frame of serial data is passed to an output of each of said routers;

a control unit having logic to control loading and startup of said routers; and

a plurality of field processing units to receive a bit-clock-out signal from each of said routers and serial data from the communication line, each of said field processing units splitting the frame of serial data into component fields and performing processing on the component fields, wherein the control unit receives a bus signal, a frame start signal, and a bit-clock-in signal.

9. (Cancelled)

10. (Original) The programmable frame splitter according to claim 8, wherein the component fields include voice, video and data.

11. (Original) The programmable frame splitter according to claim 8, wherein the logic to specify which bits of the frame of serial data is passed to the output of each of said routers is implemented utilizing at least one memory device.

12. (Original) The programmable frame splitter according to claim 11, wherein

the logic is implemented with a N x 1 memory device and an address counter, where N is a number of bits equal to the largest possible frame size.

13. (Original) The programmable frame splitter according to claim 11, wherein the logic is implemented with a N bit register and a N bit shift register, where N is a number of bits equal to the largest possible frame size.

14. (Currently Amended) A program code storage device, comprising:

a machine-readable storage medium; and

machine-readable program code, stored on the machine-readable storage medium, which when executed causes a control unit ~~having instructions~~ to receive a bus signal, a frame start signal, and a bit-clock-in signal, write data received from a bus into a router table of a plurality of programmable routers, initiate startup of the plurality of programmable routers, determine which bits of a frame of serial data is passed to an output of each of the routers as a bit-clock-out signal; and

process the bit-clock-out signal from each of said routers and serial data from a communication line, wherein the frame of serial data is split into component fields.

15. (Original) The program code storage device according to claim 14, wherein each of the programmable routers operates independently and is programmable on a bit-by-bit basis to pass any combination of frame bits, and each one of the routers contains a table of data, received from a control unit via the bus, said data specifying which bits of the frame is passed to each of the routers' output as the bit-clock-out signal.

16. (Currently Amended) The ~~machine-readable~~ program code storage device according to claim 14, wherein the router table is implemented with a N x 1 memory

device and an address counter, where N is a number of bits equal to a largest possible frame size.

17. (Currently Amended) The ~~machine-readable~~ program code storage device according to claim 14, wherein the router table is implemented with a N bit register and a N bit shift register, where N is a number of bits equal to a largest possible frame size.

18. (Currently Amended) The ~~machine-readable~~ program code storage device according to claim 14, wherein the router table is implemented utilizing at least one memory device.

19. (Previously Presented) A programmable frame splitting system, comprising:

a communication line;

a plurality of programmable routers connected to said communication line, wherein each of said routers contains logic to specify which bits of a frame of serial data is passed to an output of each router;

a control unit containing logic to control loading and startup of said routers; and

a plurality of field processing units to receive a bit clock out signal from each of said routers and serial data from the communication line, wherein each of said field processing units splits the frame of serial data into component fields and performs processing on the component fields, wherein the control unit receives a bus signal, a frame start signal, and a bit-clock-in signal.

20. (Cancelled)

21. (Original) The programmable frame splitting system according to claim 19, wherein the component fields include voice, video and data.

22. (Original) The programmable frame splitter system according to claim 19, wherein the logic to specify which bits of the frame of serial data is passed to the output of each of said routers is implemented utilizing at least one memory device.

23. (Original) The programmable frame splitter according to claim 22, wherein the logic is implemented with a N x 1 memory device and an address counter, where N is a number of bits equal to the largest possible frame size.

24. (Original) The programmable frame splitter according to claim 22, wherein the logic is implemented with a N bit register and a N bit shift register, where N is a number of bits equal to the largest possible frame size.

25. (Previously Presented) A method of programmable frame splitting, comprising:

receiving a bus signal, a frame start signal, and a bit-clock-in signal;

writing data received from a bus into a router table of a plurality of programmable routers, initiating startup of the plurality of programmable routers;

determining which bits of a frame of serial data is passed to an output of each of the routers as a bit-clock-out signal; and

processing the bit-clock-out signal from each of said routers and serial data from the communication line, wherein the frame of serial data is split into component fields and each component field is processed.

26. (Original) The method according to claim 25, wherein each of the programmed routers operates independently and is programmable on a bit-by-bit basis to pass any combination of frame bits, wherein each one of the routers contains a table of data, received from a control unit via the bus, said data specifying which bits of the

frame is passed to each of the routers' output as the bit-clock-out signal.

27. (Original) The method according to claim 26, wherein the table is implemented with a N x 1 memory device and an address counter, where N is a number of bits equal to a largest possible frame size.

28. (Original) The method according to claim 26, wherein the table is implemented with a N bit register and a N bit shift register, where N is a number of bits equal to a largest possible frame size.

29. (Original) The method according to claim 26, wherein the table is implemented utilizing at least one memory device.

30. (Original) The method according to claim 25, wherein the determining of which bits of the frame is passed to each of the routers' output as the bit-clock-out signal, at start of each frame an address counter is reset to zero and then increments at each bit time, as the address increments a next table value is read, and a value of one causes the bit-clock-in signal to be passed as the bit-clock-out signal, while a value of zero causes the bit-clocked-out signal to be negated.